

In the claims:

Please substitute the following full listing of claim for the claims as originally filed or most recently amended. Claims 33, 35 - 37 and 42 - 44 are currently canceled without prejudice or disclaimer.

ECT must be integrated form
1. (Currently Amended) An ^{emitter turn-off} [emitter controlled] thyristor device package having a cathode terminal and an anode terminal, comprising:

a thyristor device having a thyristor emitter, a thyristor collector, and a thyristor gate, said thyristor comprising alternating P-type and N-type semiconductor regions;

1.2 1st [a first discrete metal oxide semiconductor (MOS) transistor] ~~(MOS)~~ connected in series with said thyristor between said cathode terminal and and said thyristor emitter;

fig. 11.2 1st [a second discrete MOS transistor] connected between said cathode terminal and said thyristor gate, a gate terminal of said second MOS transistor connected to said cathode terminal; and

means for injecting electrons into said thyristor for triggering said thyristor into a a latching state;

wherein a first voltage applied to a gate terminal of said first MOS transistor causes a forward current to flow between said cathode terminal and said anode

ant. basis, 21 terminal turning said [emitter controlled] thyristor device to an on state, and a zero to second voltage applied to said gate of said first MOS transistor turns

ant. basis, 24 said emitter [controlled thyristor] device to an off state.

2. (Currently Amended) An emitter controlled thyristor device package as recited in claim 1 further comprises comprising a floating ohmic contact (FOC) for shorting said emitter and a source terminal of said first MOS transistor.

3. (Currently Amended) An emitter controlled thyristor device package as recited in claim 1 further ~~comprises~~ comprising a metal strap ~~to~~ for shorting said thyristor emitter and a source terminal of said first MOS transistor.

112 1st
fig. 10
4. (Currently Amended) An emitter controlled thyristor device package as recited in claim 1, further comprising:

a third MOS transistor having a source and a drain connected between said thyristor emitter and a thyristor lower base region, and

a gate connected to said cathode terminal.

Cont
D
fig. 10
112 1st
5. (Currently Amended) An emitter controlled thyristor device package as recited in claim 1 wherein said first MOS transistor comprises a PMOS transistor, and said second MOS transistor comprises a PMOS transistor.

112 1st
fig. 10
6. (Currently Amended) An emitter controlled thyristor device package as recited in claim 4 wherein said first MOS transistor comprises a PMOS transistor, said second MOS transistor comprises a PMOS transistor, and said third MOS transistor comprises an NMOS transistor.

112 1st
fig. 4B
7. (Currently Amended) An emitter controlled thyristor device package as recited in claim 4 wherein said first MOS transistor comprises a NMOS transistor, said second MOS transistor comprises a PMOS transistor, and said third MOS transistor comprises an NMOS transistor.

8. (Currently Amended) An emitter controlled thyristor device package as recited/in claim 4, further comprising

a metal strap for shorting said thyristor emitter with one of a drain and source terminal of said first MOS transistor.

112 1st
fig. 2B
9. (Currently Amended) An emitter controlled thyristor device package as recited in claim 1, further comprising

a diode connected between said gate of said first MOS transistor and said thyristor emitter.

10. - 18. (Previously canceled)

19. (Currently Amended) A ^{ETO}[gate turn-off (GTO)] thyristor device package comprising:

a first metal plate;

a second metal plate;

a third metal plate electrically insulated from said second metal plate;

fig. 17A, 17B
a thyristor sandwiched between said first metal plate and said second metal plate, a collector of said thyristor contacting said first metal plate acting as an anode for said GTO thyristor device package;

a first discrete metal oxide semiconductor (MOS) transistor positioned on said second metal plate adjacent said thyristor, said first MOS transistor having a first terminal connected to an emitter of said thyristor and a second terminal connected to said third metal plate acting as a cathode for said GTO device package; and

a second discrete MOS transistor positioned on said second metal plate adjacent said thyristor, said second MOS transistor having a first terminal connected to a gate of said thyristor, said second MOS transistor further having a second terminal and a gate terminal

connected to said third metal plate,

wherein a first voltage applied to a gate terminal of said first MOS transistor turns said thyristor to an on state causing a current to flow between said cathode and said anode, and a zero to second voltage applied to said gate of said first MOS transistor turns said ~~emitter controlled~~ thyristor device to an off state.

20. (Currently Amended) A ^{ETO} [gate turn-off (GTO)] thyristor device package as recited in claim 19, further comprising a clamp means for holding said first, second and third metal ~~layers~~ plates together.

21. (Previously Amended) A ^{ETO} [gate turn-off (GTO)] thyristor device package as recited in claim 19, wherein said first, second and third metal plates comprise copper plates.

22. (Currently Amended) A [gate turn-off (GTO) thyristor device package] as recited in claim ~~39~~ 19, wherein [said first and second discrete semiconductor switches] are first and second MOS transistors, respectively, and said first MOS transistor and said second MOS transistor are complementary.

23. (Currently Amended) A ^{ETO} [gate turn-off thyristor (GTO)] device package comprising:

a gate turn-off (GTO) thyristor comprising a thyristor gate, a thyristor emitter, and a thyristor collector forming an anode terminal;

a first plurality of discrete switching devices connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of ^{each of} said MOS ~~transistors~~ ^{1st plurality of} discrete switching devices connected to said thyristor emitter and a second terminal of ^{each of} said ~~MOS transistors~~ ^{1st plurality of} discrete switching devices connected to a cathode terminal of said GTO device package; and

figs. 17A-17D

a second plurality of discrete switching devices connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of ^{each of} said ~~MOS~~ switching devices connected to said thyristor gate and a second terminal of ^{each of} said switching devices connected to said cathode terminal of said GTO device package,

wherein a first voltage applied to a gate terminal of ^{each of} said first plurality of switching devices turns said GTO thyristor to an on state causing a current to flow between said cathode terminal and said anode terminal, and a zero to second voltage applied to said gate ^{terminal of each} of said first plurality of switching devices turns said GTO thyristor to an off state.

ETO

24. (Previously Amended) A [gate turn-off thyristor (GTO)] device package as recited in claim 23, further comprising:

a first metal plate forming said cathode terminal;
a second metal plate separated from said first metal plate by an insulation layer, wherein said GTO thyristor and said ^{1st and 2nd plurality of} [MOS transistors and said] switching devices are positioned on said second metal plate, said first and second metal plates acting as a heat sink.

25. (Previously Amended) A [gate turn-off thyristor (GTO)] device package as recited in claim 23 further comprising a third metal plate forming an anode terminal of said GTO thyristor device package.

26. (Currently Amended) A [gate turn-off thyristor (GTO)] ^{2nd plurality of} device package as recited in claim 23 wherein said discrete switching devices each comprise a MOSFET MOS transistor having a gate connected to said cathode terminal.

amended
fig. 18
3 each of ^{2nd plurality of discrete} said switching devices comprise a diode.

27. (Previously Amended) A [gate turn-off thyristor (GTO)] device package as recited in claim 23 wherein

amended
fig. 18
3 each of ^{2nd plurality of discrete} said switching devices comprise a diode connected in parallel with a capacitor.

28. (Previously Amended) A [gate turn-off thyristor (GTO)] device package as recited in claim 23 wherein

amended
fig. 18
3 each of ^{2nd plurality of discrete} said switching devices comprise a Zener diode connected in parallel with a capacitor.

29. (Previously Amended) A [gate turn-off thyristor (GTO)] device package as recited in claim 23 wherein

amended
fig. 18
Cont. D
fig. 19
3 each of ^{2nd plurality of discrete} said switching devices comprise a transistor connected in parallel with a capacitor.

30. (Previously Amended) A [gate turn-off thyristor (GTO)] device package as recited in claim 23 wherein

31. (Currently Amended) A [gate turn-off thyristor (GTO)] device package as recited in claim 26 further comprising;

fig. 18
5 a first feedback path connecting said gate terminal of [said MOS transistors] to said thyristor emitter; and

8 a second feedback path connecting said gate terminal of [said MOS transistors] to said thyristor gate terminal through a diode.

fig. 19
2 32. (Currently Amended) A [gate turn-off thyristor (GTO)] as recited in claim 23, further wherein ^{each of plurality of discrete} said first switching devices comprise a MOS transistor comprising:

4 a feedback path connecting [said] gate terminal of said MOS transistor to said thyristor emitter;

6 a capacitor connected in parallel to [said MOS switching device] connecting [said second terminal of

8 said MOS transistor] to said thyristor gate terminal.

33. - 37. (Currently Canceled)

38. (Currently Amended) An emitter turn-off thyristor
~~as recited in claim 33, device package including~~

a thyristor element having an anode terminal, an
emitter terminal and a gate terminal,

a first discrete semiconductor switch connected in
series with said emitter terminal of said thyristor
device by a first terminal of said first semiconductor
switch,

a second discrete semiconductor switch connected
in series with said gate terminal of said thyristor
device by a first terminal of said second discrete
semiconductor switch; second terminals of said first
and second discrete semiconductor switches being
connected together, and

means for shorting said emitter of said thyristor
element to a terminal of said first discrete
17 semiconductor switch^{delete} [or] for injecting electrons into
said thyristor for triggering said thyristor into a
latching state;

wherein said first and second discrete
semiconductor switches are arranged such that a signal
of a first type applied to said first discrete
23 ^{semiconductor} [electronic] switch turns said emitter turn-off thyristor
to an on-state and a signal of a second type applied to
25 said first ^{discrete semiconductor} [electronic] switch turns said ^{delete} [emitter turn-
26 off] thyristor to an off-state, and

wherein at least one of said first and second
semiconductor switches is constituted by a plurality of
semiconductor devices.

39. - 41. (Previously Canceled)

42. - 44. (Currently Canceled)